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(54) PIXEL CIRCUIT OF DISPLAY PANEL, METHOD OF CONTROLLING THE PIXEL CIRCUIT, AND ORGANIC LIGHT EMITTING DISPLAY INCLUDING THE DISPLAY PANEL

(76) Inventors: **Bo-Yong Chung**, Yongin-city (KR); **Keum-Nam Kim**, Yongin-city (KR)

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(57) **ABSTRACT**

A pixel circuit of a display panel, a method of driving the pixel circuit, and an organic light emitting display device including the display panel are provided. All of a plurality of transistors used in the pixel circuit are NMOS transistors, and the pixel circuit is configured to compensate for a voltage change at a source electrode of a driving transistor during light emission.

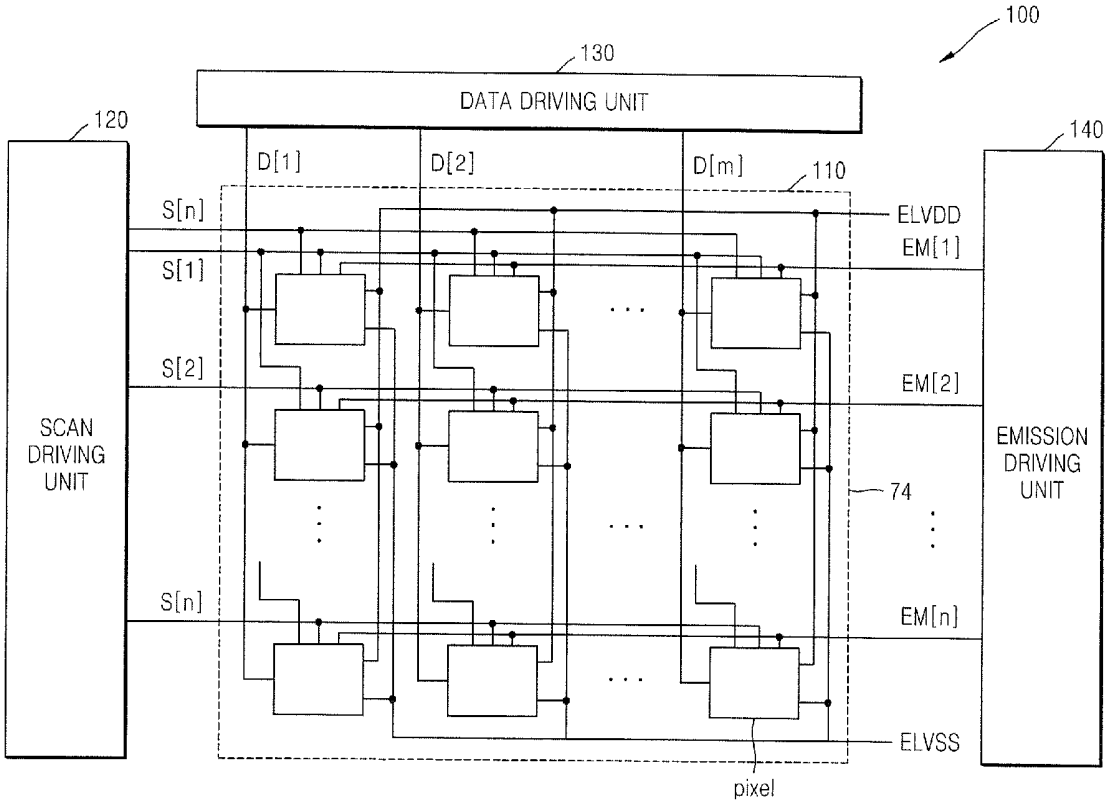


FIG. 1

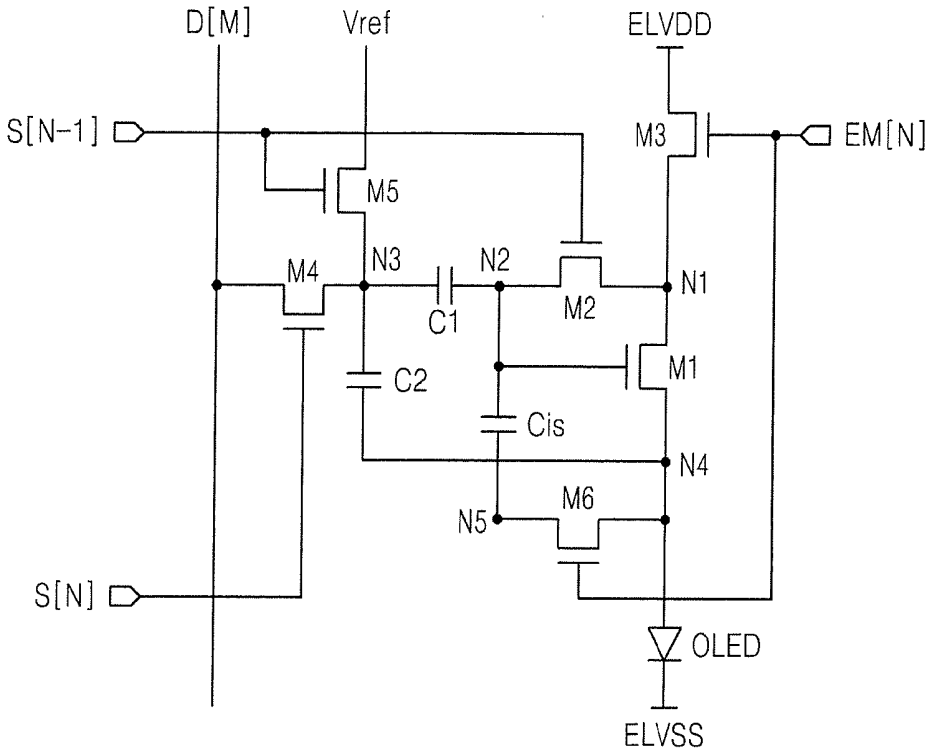

D[M]
Vref
ELVDD
S[N-1]
M3
EM[N]
M5
M4
N3
N2
N1
C1
M2
M1
C2
Cis
N4
N5
M6
S[N]
OLED
ELVSS

FIG. 2

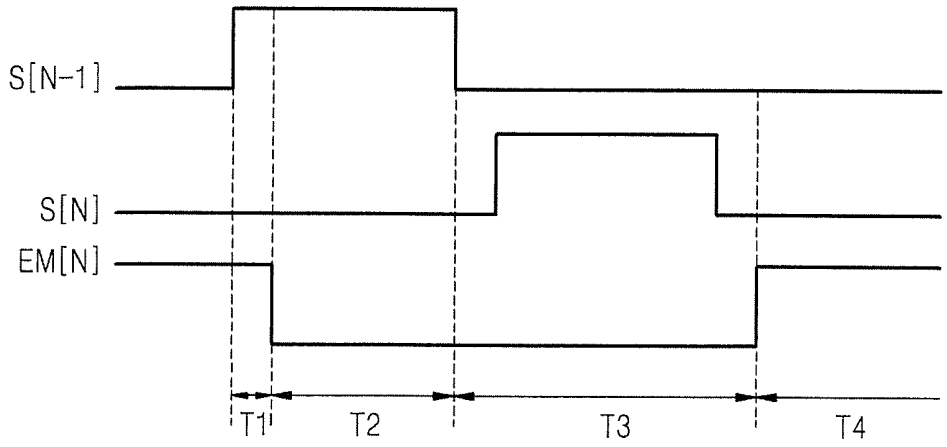

S[N-1]
S[N]
EM[N]
T1
T2
T3
T4

FIG. 3

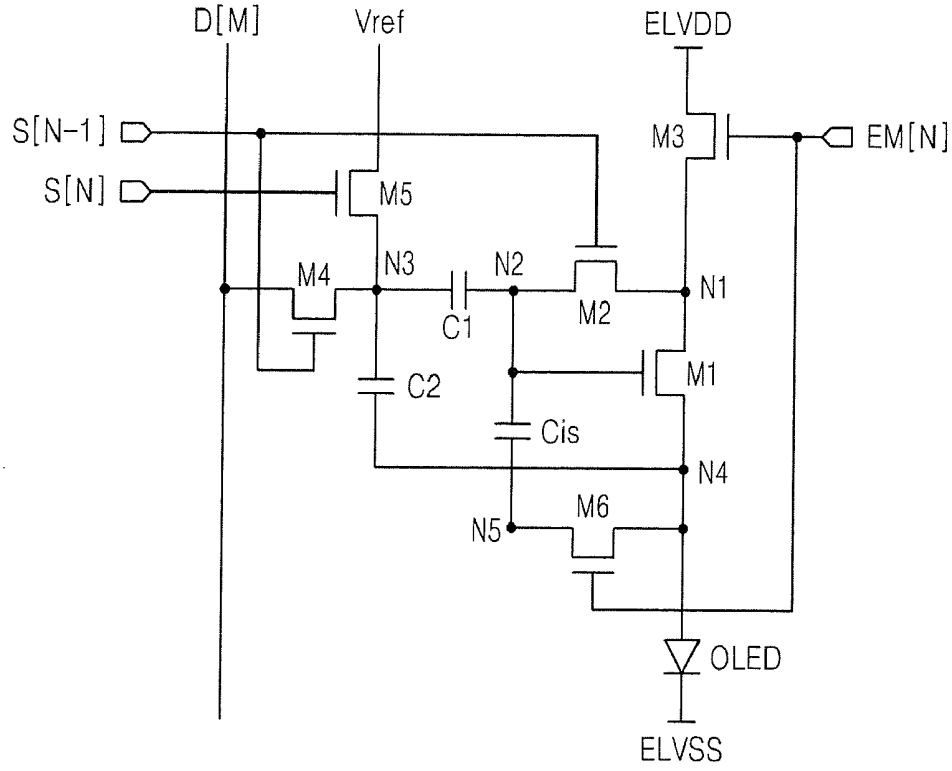

D[M]
Vref
ELVDD
S[N-1]
S[N]
M3
EM[N]
M5
M4
N3
N2
N1
C1
M2
C2
M1
Cis
N4
N5
M6
OLED
ELVSS

FIG. 4

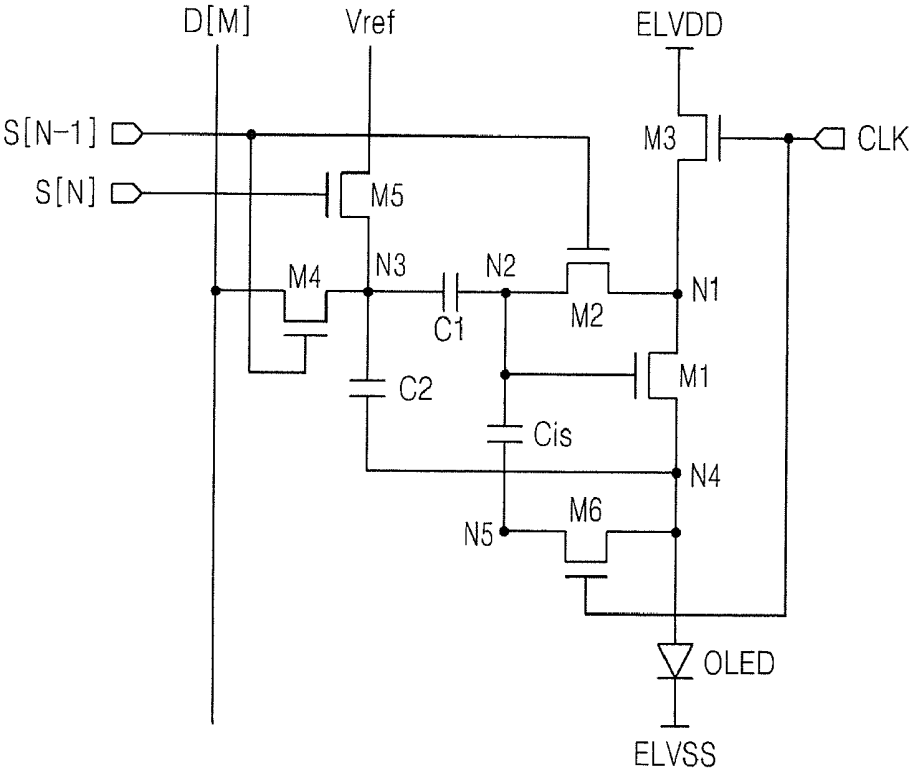

D[M]
Vref
ELVDD
S[N-1]
S[N]
M3
CLK
M5
M4
N3
N2
N1
C1
M2
C2
M1
Cis
N4
N5
M6
OLED
ELVSS

FIG. 5

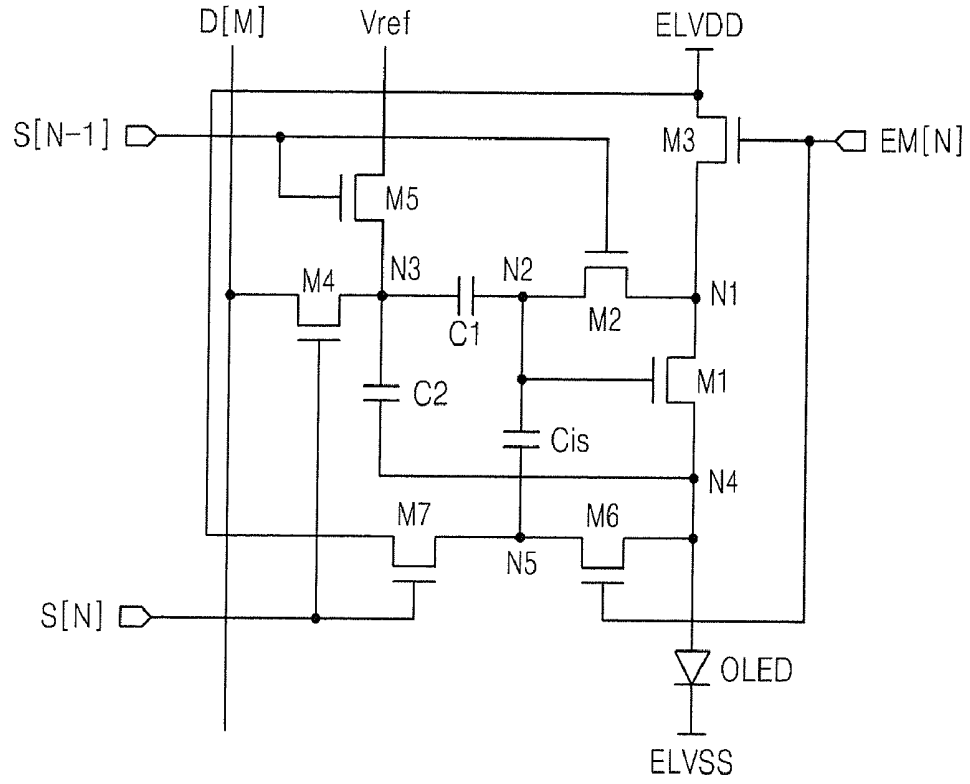

D[M]
Vref
ELVDD
S[N-1]
M3
EM[N]
M5
M4
N3
N2
N1
C1
M2
C2
M1
Cis
N4
M7
M6
N5
S[N]
OLED
ELVSS

FIG. 6

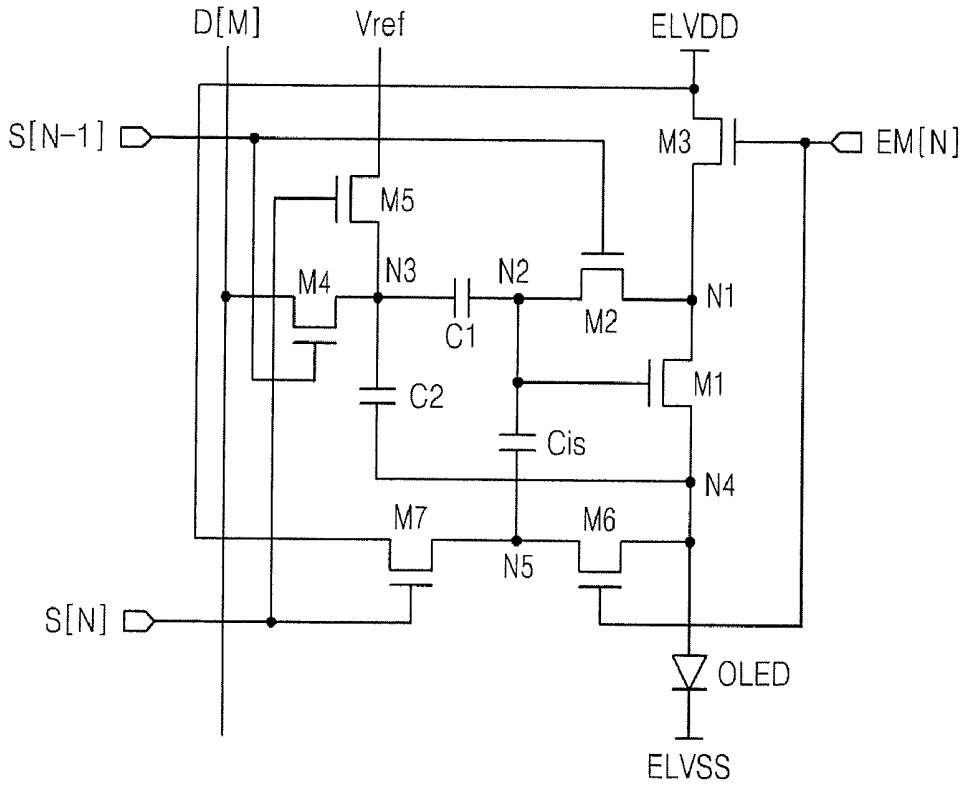

D[M]
Vref
ELVDD
S[N-1]
M3
EM[N]
M5
M4
N3
N2
N1
C1
M2
C2
M1
Cis
N4
M7
M6
N5
S[N]
OLED
ELVSS

FIG. 7

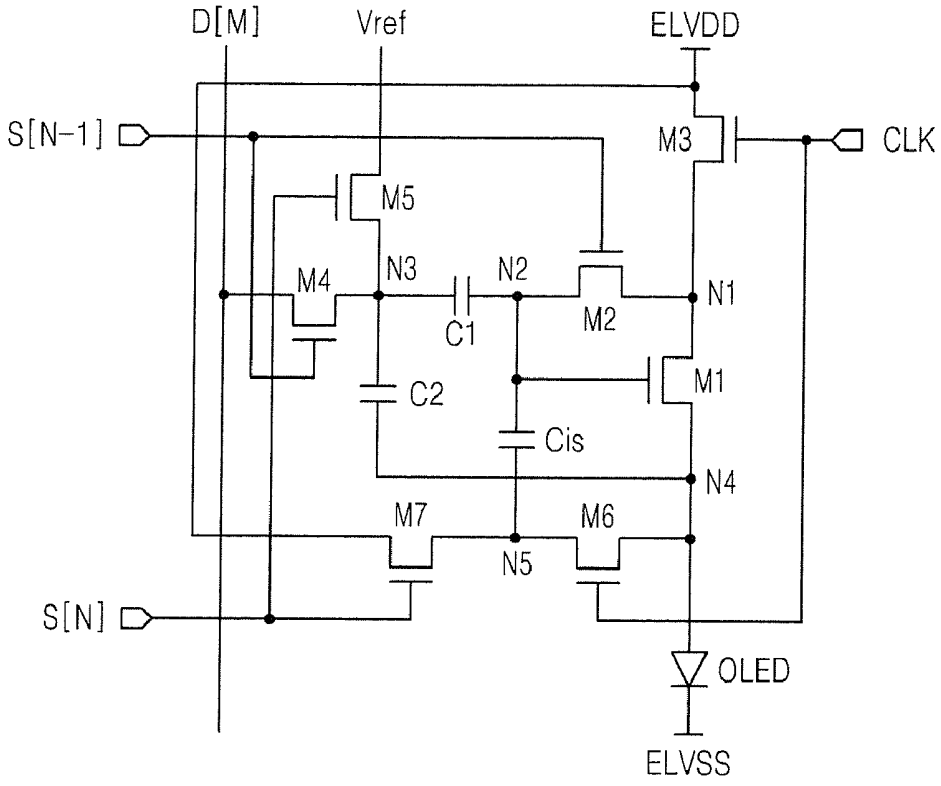
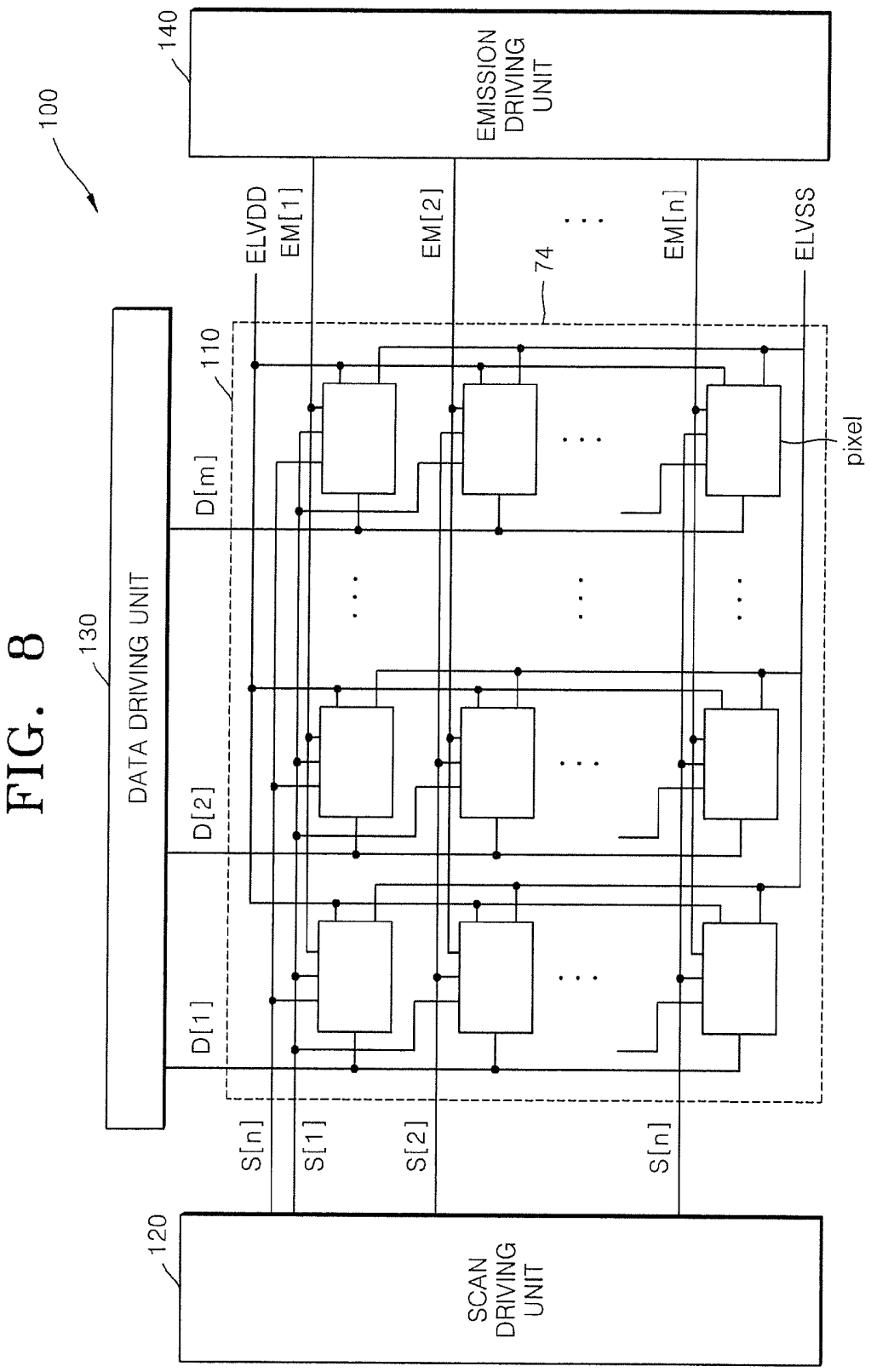

D[M]
Vref
ELVDD
S[N-1]
M3
CLK
M5
M4
N3
N2
N1
C1
M2
C2
M1
Cis
N4
M7
M6
N5
S[N]
OLED
ELVSS

FIG. 8


100
140
EMISSION DRIVING UNIT
ELVDD
EM[1]
EM[2]
EM[n]
ELVSS
74
110
130
DATA DRIVING UNIT
D[m]
D[2]
D[1]
pixel
S[n]
S[1]
S[2]
S[n]
120
SCAN DRIVING UNIT

PIXEL CIRCUIT OF DISPLAY PANEL, METHOD OF CONTROLLING THE PIXEL CIRCUIT, AND ORGANIC LIGHT EMITTING DISPLAY INCLUDING THE DISPLAY PANEL

CROSS-REFERENCE TO RELATED PATENT APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2009-0089646, filed on Sep. 22, 2009, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] 1. Field

[0003] An aspect of an embodiment of the present invention relates to a pixel circuit of a display panel, a method of driving the pixel circuit, and an organic light emitting display device including the display panel.

[0004] 2. Description of Related Art

[0005] Display devices receive image data from an external source and display images corresponding to the image data. Examples of the display devices include cathode ray tubes (CRTs), field emission displays (FEDs), liquid crystal displays (LCDs), and plasma display panels (PDPs).

[0006] Organic light emitting display devices using organic light emitting diodes (OLEDs) as organic light emitting devices have been recently developed and are being used in some products. In such organic light emitting display devices, a display panel includes a plurality of pixel circuits, and images may be displayed on the display panel by controlling the light emission of an OLED included in each of the pixel circuits. The pixel circuits included in the display panel affect the quality of display of the organic light emitting display devices. Much research into the structure of pixel circuits and driving methods thereof are being conducted.

SUMMARY

[0007] An aspect of an embodiment of the present invention provides a pixel circuit of a display panel, capable of compensating for a voltage change at a source electrode of a driving transistor during light emission, a method of driving the pixel circuit, and an organic light emitting display device including the display panel.

[0008] According to an embodiment of the present invention, there is provided a pixel circuit for a display panel, including an organic light emitting diode (OLED) including an anode and a cathode; a first NMOS transistor including a first electrode coupled to a first node, a second electrode coupled to the anode of the OLED, and a gate electrode coupled to a second node; a second NMOS transistor including a first electrode coupled to the second node, a second electrode coupled to the first node, and a gate electrode; a third NMOS transistor including a first electrode coupled to a first power source, a second electrode coupled to the first node, and a gate electrode; a fourth NMOS transistor including a first electrode coupled to a data line, a second electrode coupled to a third node, and a gate electrode; a fifth NMOS transistor including a first electrode coupled to a reference power source, a second electrode coupled to the third node, and a gate electrode; a sixth NMOS transistor including a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode; a first capacitor coupled between the second node and the third node; a second capacitor coupled between the third node and the anode of the OLED; and a third capacitor coupled between the second node and the first electrode of the sixth NMOS transistor.

[0009] The gate electrode of the second NMOS transistor and the gate electrode of the fifth NMOS transistor may be configured to receive a previous scan signal.

[0010] The gate electrode of the fourth NMOS transistor may be configured to receive a current scan signal.

[0011] The gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor may be configured to receive an emission signal.

[0012] The pixel circuit may further include a seventh NMOS transistor including a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode configured to receive the current scan signal.

[0013] The reference power source may have a ground voltage.

[0014] The gate electrode of the second NMOS transistor and the gate electrode of the fourth NMOS transistor may be configured to receive a previous scan signal.

[0015] The gate electrode of the fifth NMOS transistor may be configured to receive a current scan signal.

[0016] The gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor may be configured to receive an emission signal.

[0017] The gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor may be configured to receive an external clock signal.

[0018] The pixel circuit may further include a seventh NMOS transistor including a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode configured to receive the current scan signal.

[0019] The reference power source may have a logic high signal.

[0020] The first electrode of the first NMOS transistor may be a drain electrode and the second electrode of the first NMOS transistor may be a source electrode.

[0021] Capacitances of the first and second capacitors may be greater than capacitance of the third transistor.

[0022] According to another embodiment of the present invention, there is provided a method of driving a pixel circuit including an OLED having an anode and a cathode, a driving transistor, a plurality of switching transistors, a booster transistor having a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode, a plurality of capacitors, and a booster capacitor coupled between the gate electrode of the driving transistor and the first electrode of the booster transistor, wherein the driving transistor, the plurality of switching transistors and the booster transistor are NMOS transistors. The method includes turning on the booster transistor when a previous scan signal and a current scan signal are logic low and an emission signal is logic high, and transmitting a voltage change at the anode of the OLED to the gate electrode of the driving transistor via coupling of the booster capacitor.

[0023] The voltage change at the anode of the OLED may correspond to a voltage difference between a voltage at the anode when substantially no current flows through the OLED and a voltage at the anode when a current flows through the OLED.

[0024] The method may further include initializing the pixel circuit when the previous scan signal and the emission signal are logic high and the current scan signal is logic low.

[0025] The method may further include diode-connecting the driving transistor to compensate for a threshold voltage of the OLED when the previous scan signal is logic high and the current scan signal and the emission signal are logic low.

[0026] The method may further include performing data writing when the previous scan signal and the emission signal are logic low and the current scan signal is logic high.

[0027] According to another embodiment of the present invention, there is provided an organic light emitting display device including a scan driver for providing scan signals to a plurality of scan lines; an emission driver for providing emission signals to a plurality of emission control lines; a data driver for providing data signals to a plurality of data lines; and a plurality of pixel circuits at crossing regions between the scan lines, the emission control lines, and the data lines. Each of the pixel circuits includes an OLED including an anode and a cathode; a first NMOS transistor including a first electrode coupled to a first node, a second electrode coupled to the anode of the OLED, and a gate electrode coupled to a second node; a second NMOS transistor including a first electrode coupled to the second node, a second electrode coupled to the first node, and a gate electrode; a third NMOS transistor including a first electrode coupled to a first power source, a second electrode coupled to the first node, and a gate electrode; a fourth NMOS transistor including a first electrode coupled to a data line, a second electrode coupled to a third node, and a gate electrode; a fifth NMOS transistor including a first electrode coupled to a reference power source, a second electrode coupled to the third node, and a gate electrode; a sixth NMOS transistor including a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode; a first capacitor coupled between the second node and the third node; a second capacitor coupled between the third node and the anode of the OLED; and a third capacitor coupled between the second node and the first electrode of the sixth NMOS transistor.

[0028] The gate electrode of the second NMOS transistor and the gate electrode of the fifth NMOS transistor may be coupled to an (N−1)th scan line, wherein N is a natural number satisfying 0<N<n. The gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor may be coupled to an N-th emission control line. The gate electrode of the fourth NMOS transistor may be coupled to an N-th scan line.

[0029] The gate electrode of the second NMOS transistor and the gate electrode of the fourth NMOS transistor may be coupled to an (N−1)th scan line, wherein N is a natural number satisfying 0<N<n. The gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor may be coupled to an N-th emission control line. The gate electrode of the fifth NMOS transistor may be coupled to an N-th scan line.

[0030] The organic light emitting display device may further include a seventh NMOS transistor including a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode coupled to the N-th scan line.

[0031] The first electrode of the first NMOS transistor may be a drain electrode and the second electrode of the first NMOS transistor may be a source electrode.

[0032] Capacitances of the first and second capacitors may be greater than capacitance of the third transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The above and other features and aspects of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[0034] FIG. **1** is a circuit diagram of a pixel circuit of a display panel, according to an embodiment of the present invention;

[0035] FIG. **2** is a timing diagram for describing a method of driving the pixel circuit illustrated in FIG. **1**, according to an embodiment of the present invention;

[0036] FIG. **3** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention;

[0037] FIG. **4** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention;

[0038] FIG. **5** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention;

[0039] FIG. **6** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention;

[0040] FIG. **7** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention; and

[0041] FIG. **8** is a block diagram of an organic light emitting display device according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0042] Hereinafter, embodiments of the present invention will be described in detail by explaining various embodiments of the invention with reference to FIGS. **1** through **8**. Here, when a first element is described as being coupled or connected to a second element, the first element may be directly coupled to the second element or indirectly coupled to the second element via a third element.

[0043] FIG. **1** is a circuit diagram of a pixel circuit of a display panel, according to an embodiment of the present invention.

[0044] Referring to FIG. **1**, the pixel circuit according to one embodiment includes an organic light emitting diode (OLED), a driving transistor (a first transistor M**1**), a plurality of switching transistors (second through sixth transistors M**2** through M**6**), and a plurality of capacitors (first through third capacitors C**1**, C**2** and Cis), and all of the transistors included in the pixel circuit are NMOS transistors. In the display panel, a plurality of the pixel circuits may be arranged in an n×m matrix. The pixel circuit illustrated in FIG. **1** corresponds to a pixel circuit located in an N-th row and an M-th column.

[0045] The OLED includes an anode and a cathode, wherein the cathode is connected to a second power source. The OLED generates light by using a current generated by the driving transistor. The brightness of the light depends on the magnitude of the current flowing through the OLED.

[0046] Referring to FIG. **1**, the first transistor M**1** includes a first electrode connected to a first node N**1**, a second electrode connected to the anode of the OLED, and a gate electrode connected to a second node N**2**. The first electrode of the

first transistor M1 may be a drain electrode, and the second electrode of the first transistor M1 may be a source electrode. The first transistor M1 operates as the driving transistor, and generates a current depending on a voltage Vgs between the gate electrode and the source electrode and outputs the current to the OLED. Hereinafter, the terms "first transistor" and "driving transistor" will be used interchangeably.

[0047] The second transistor M2 includes a first electrode connected to the second node N2 and a second electrode connected to the first node N1. The second transistor M2 also includes a gate electrode to which an external control signal is applied. The second transistor M2 is connected between the first electrode and the gate electrode of the driving transistor M1, and when the second transistor M2 is turned on by the external control signal, the second transistor M2 connects the driving transistor M1 to be in a diode connection (or diode-connected) state. The diode connection of the driving transistor M1 may compensate for a threshold voltage Vth of the driving transistor M1 and a threshold voltage Vto of the OLED, which is present between the anode and the cathode of the OLED during non-emission. The external control signal corresponds to a previous scan signal, which is a scan signal provided from an (N−1)th scan line S[N−1] that is a previous scan line. Thus, the gate electrode of the second transistor M2 is connected to the previous scan line S[N−1].

[0048] The third transistor M3 includes a first electrode connected to a first power source and a second electrode connected to the first node N1. The third transistor M3 also includes a gate electrode to which an external control signal is applied. When the third transistor M3 is turned on according to the external control signal, the third transistor M3 applies a first power supply voltage ELVDD to the first electrode of the driving transistor M1. Since the third transistor M3 is turned on, a current is generated by the driving transistor M1, and the current flows to the OLED. The external control signal is an emission signal and is provided from an N-th emission control line EM[N]. Thus, the gate electrode of the third transistor M3 is connected to the N-th emission control line EM[N].

[0049] The fourth transistor M4 includes a first electrode connected to an M-th data line D[M] and a second electrode connected to a third node N3. The fourth transistor M4 also includes a gate electrode to which an external control signal is applied. When the fourth transistor M4 is turned on according to the external control signal, a data voltage Vdata provided from the M-th data line D[M] is applied to the third node N3. The external control signal is a current scan signal provided from an N-th scan line S[N], that is a current scan line. Thus, the gate electrode of the fourth transistor M4 is connected to the current scan line S[N].

[0050] The fifth transistor M5 includes a first electrode connected to a reference power source and a second electrode connected to the third node N3. The fifth transistor M5 also includes a gate electrode to which an external control signal is applied. When the fifth transistor M5 is turned on according to the external control signal, a reference voltage Vref provided from the reference power source is applied to the third node N3. The external control signal may be the previous scan signal that is applied to the gate electrode of the second transistor M2. Thus, the gate electrode of the fifth transistor M5 is connected to the previous scan line S[N−1].

[0051] The sixth transistor M6 includes a first electrode connected to the third capacitor Cis and a second electrode connected to the anode of the OLED. The sixth transistor M6 also includes a gate electrode to which an external control signal is applied. When the sixth transistor M6 is turned on according to the external control signal, a voltage of the anode of the OLED is applied to one terminal of the third capacitor Cis. The external control signal may be the emission signal that is applied to the gate electrode of the third transistor M3. Thus, the gate electrode of the sixth transistor M6 is connected to the N-th emission control line EM[N].

[0052] The second through sixth transistors M2 through M6 serve as the switching transistors.

[0053] The first capacitor C1 includes a first terminal connected to the third node N3 and a second terminal connected to the second node N2.

[0054] The second capacitor C2 includes a first terminal connected to the third node N3 and a second terminal connected to the anode of the OLED.

[0055] The third capacitor Cis includes a first terminal connected to the second node N2 and a second terminal connected to the first electrode of the sixth transistor M6, which is connected to the fifth node N5. When the sixth transistor M6 is turned on according to the emission signal, the voltage of the anode of the OLED is applied to the second terminal of the third capacitor Cis. Due to the coupling of capacitors, a voltage change at the first terminal of the third capacitor Cis, which is connected to the gate electrode of the driving transistor M1, corresponds to a voltage change at the second terminal of the third capacitor Cis.

[0056] When a capacitance of the first capacitor C1 is c1, a capacitance of the second capacitor C2 is c2, and a capacitance of the third capacitor Cis is cis, a condition of c1>>cis, c2>>cis is satisfied.

[0057] The first power source provides the first power supply voltage ELVDD, and the second power source provides a second power supply voltage ELVSS. The second power supply voltage ELVSS may be a ground voltage GND. The reference power source may provide a reference voltage Vref, which may be a ground voltage GND.

[0058] As described above, all of the transistors included in the pixel circuit according to the described embodiment are NMOS transistors. In a conventional pixel circuit, PMOS transistors may be used. Since crystalline silicon is used to manufacture PMOS-type thin film transistors (TFTs), an Excimer Laser Annealing (ELA) device, which is a crystallization device, is used.

[0059] However, when a pixel circuit uses NMOS transistors, the following characteristics exist.

[0060] First, a TFT may be manufactured using amorphous silicon (a-Si), and thus an ELA device, which is expensive, is not used.

[0061] Second, the number of masks used may be reduced when a pixel circuit using NMOS transistors is produced, compared with when a pixel circuit using PMOS transistors is produced.

[0062] Third, when NMOS transistors are used, it is possible to use oxide TFTs. When oxide TFTs are used, voltage uniformity, which is a characteristic of amorphous silicon, and a high electron mobility, which is a characteristic of Low-Temperature Poly-Silicon (LTPS), can be achieved. This facilitates an improvement of the life span of a display panel and realization of a high resolution.

[0063] In the case of LCDs, pixel circuits are manufactured by using only NMOS transistors. Thus, equipment for manufacturing LCDs may be used in manufacturing the pixel circuit according to an embodiment of the present invention, resulting in cost savings.

[0064] An operation of the pixel circuit of FIG. **1** will now be described with reference to FIG. **2**.

[0065] FIG. **2** is a timing diagram for describing a method of driving the pixel circuit illustrated in FIG. **1**, according to one embodiment.

[0066] Overall operation of the pixel circuit is divided into first through fourth intervals T**1** through T**4**. An operation of the pixel circuit in each of the first through fourth intervals T**1** through T**4** will now be described.

[0067] In the first interval T**1**, initialization is performed.

[0068] In the first interval T**1**, the previous scan signal is supplied to the previous scan line S[N−1], and the emission signal is supplied to the emission control line EM[N]. In other words, the previous scan signal and the emission signal are logic high in the first interval T**1**. The second, third, fifth, and sixth transistors M**2**, M**3**, M**5**, and M**6** are turned on by the previous scan signal and the emission signal, and thus each node of the pixel circuit is initialized. Here, the current scan signal applied to the current scan line S[N] is logic low.

[0069] In the second interval T**2**, the driving transistor M**1** is diode-connected to compensate for the threshold voltage Vto of the OLED and the threshold voltage Vth of the driving transistor M**1**.

[0070] In the second interval T**2**, the previous scan signal is logic high, and the current scan signal and the emission signal are logic low. According to the previous scan signal, the second and fifth transistors M**2** and M**5** are turned on. Since the anode of the OLED is connected to the fourth node N**4** and the threshold voltage of the OLED is Vto, a voltage Vn**4** of the fourth node N**4** is ELVSS+Vto. Since the driving transistor M**1** is diode-connected, a voltage Vn**2** of the second node N**2** is ELVSS+Vto+Vth. A voltage Vn**3** of the third node N**3** becomes the reference voltage Vref. A voltage Vn**5** of the fifth node N**5** becomes ELVSS+Vto. The voltages of the second to fifth nodes N**2** to N**5** of the pixel circuit in the second interval T**2** are summarized as follows.

$N2$: $Vn2=ELVSS+Vto+Vth$

N3: Vn3=Vref

$N4$: $Vn4=ELVSS+Vto$

$N5$: $Vn5=ELVSS+Vto$

[0071] In the third interval T**3**, data writing is performed.

[0072] In the third interval T**3**, the current scan signal is logic high, and the previous scan signal and the emission signal are logic low. When the fourth transistor M**4** is turned on by the current scan signal, the data voltage Vdata is applied to the third node N**3**. Since the fifth node N**5** is in a floating state, a voltage change at the third node N**3** is reflected at the second node N**2**. The voltages of the second to fifth nodes N**2** to N**5** of the pixel circuit in the third interval T**3** are summarized as follows.

$N2$: $Vn2=ELVSS+Vto+Vth+\Delta V1=ELVSS+Vto+Vth+Vdata-Vref$

$N3$: $Vn3=Vdata(\Delta V1=Vdata-Vref)$

$N4$: $Vn4=ELVSS+Vto$

$N5$: $Vn5=ELVSS+Vto+\Delta V1=ELVSS+Vto+Vdata-Vref=ELVSS+Va$

[0073] In the fourth interval T**4**, degradation of the OLED is compensated for. The compensation for the degradation of the OLED may be achieved by accounting for the voltage change at the anode of the OLED in the voltage applied to the gate electrode of the driving transistor M**1**.

[0074] In the fourth interval T**4**, the emission signal is logic high, and the previous scan signal and the current scan signal are logic low. The third and sixth transistors M**3** and M**6** are turned on by the emission signal. Since the third transistor M**3** is turned on, a current flows through the OLED. When the OLED enters into an emission state due to the flow of the current therein, the voltage Vn**4** of the fourth node N**4**, which is connected to the anode of the OLED, is changed. When a voltage between the anode and cathode of the OLED during light emission is Voled, the voltage Vn**4** is ELVSS+Voled. The voltage Voled varies according to the degree of degradation of the OLED. When the sixth transistor M**6** is turned on, the voltages Vn**4** and Vn**5** of the fourth and fifth nodes N**4** and N**5** are changed to ELVSS+Voled, and thus the voltage Vn**2** of the second node N**2** is also changed. In other words, the third capacitor Cis and the sixth transistor M**6** serve as a boost capacitor and a boost transistor, respectively. Calculating the voltage change of the voltage Vn**2**, a voltage variation of the voltage Vn**2** depending on the voltage change of the fourth node N**4** is $\Delta V2*\{cs/(cs+cis)\}$ and a voltage variation of the voltage Vn**2** depending on the voltage change of the fifth node N**5** is $\Delta V3*\{cis/(cs+cis)\}$, where $\Delta V2=Voled-Vto$, $\Delta V3=Voled-Va$, and cs denotes a composite capacitance when the first and second capacitors C**1** and C**2** are connected to each other in series. The voltages of the second, fourth and fifth nodes N**2**, N**4** and N**5** of the pixel circuit in the fourth interval T**4** are summarized based on this calculation, as follows.

$$N2:\ Vn2 = ELVSS + Vto + Vth + Vdata - Vref +$$
$$= \Delta V2 * \{cs/(cs+cis)\} + \Delta V3 * \{cis/(cs/cis)\}$$
$$ELVSS + Vto + Vth + Vdata - Vref +$$
$$(Voled - Vto) * \{cs/(cs+cis)\} + (Voled - Va) *$$
$$\{cis/(cs+cis)\}$$

$N4$: $Vn4=ELVSS+Voled(\Delta V2=Voled-Vto)$

$N5$: $Vn5=ELVSS+Voled(\Delta V3=ELVSS+Voled-(ELVSS+Va)=Voled-Va)$

[0075] The voltage Vn**2** of the second node N**2** is the voltage of the gate electrode of the driving transistor M**1**, and the voltage Vn**4** of the fourth node N**4** is the voltage of the source electrode of the driving transistor M**1**. In view of a condition of c**1**, c**2**>>cis, cs>>cis, accordingly,

$$Vg = Vn2$$
$$\approx ELVSS + Vto + Vth + Vdata - Vref + (Voled - Vto) +$$
$$= (Voled - Va) * \{cis/cs\}$$
$$= ELVSS + Vth + Vdata - Vref + Voled +$$
$$(Voled - Va) * \{cis/cs\}$$
$$Vs = Vn4$$
$$= ELVSS + Voled.$$

[0076] A current I flowing through the OLED according to the voltages of the driving transistor M**1** is calculated as follows:

$$\begin{aligned} I &= (\beta/2)(Vgs - Vth)^2 \\ &= (\beta/2)(Vg - Vs - Vth)^2 \\ &= (\beta/2)\{ELVSS + Vth + Vdata - Vref + Voled + \\ &\quad (Voled - Va)(cis/cs) - (ELVSS + Voled) - Vth\}^2 \\ &= (\beta/2)\{Vdata - Vref + (Voled - Va)(cis/cs)\}^2, \end{aligned}$$

wherein β denotes a gain factor.

[0077] With the above-described current I flowing through the OLED, it may be known that the voltage Voled varying according to the degradation of the OLED is reflected in the current.

[0078] As described above, in the pixel circuit and the pixel circuit driving method according to the described embodiment, the voltage change of the anode of the OLED due to the degradation of the OLED may be reflected in the voltage applied at the gate electrode of the driving transistor M**1** by using the sixth transistor M**6** and the third capacitor Cis. Accordingly, display performance of the organic light emitting display device may be prevented from degrading.

[0079] Table 1 shows a result of a simulation performed on the pixel circuit of FIG. **1**.

TABLE 1

	Before degradation	After degradation
Vn5(V)	4.62	5.12
Vn2(V)	2.57	3.05

[0080] As shown in Table 1, the voltage Vn**5** increases as the OLED degrades, and the voltage Vn**2** increases as the voltage Vn**5** increases.

[0081] Table 2 shows a result of another simulation performed on the pixel circuit of FIG. **1**.

TABLE 2

	Vn2(V)	Vn4(V)	I(A)	ΔI(A)
Standard	8.72	5.97	1.01E−06	0.00E+00
Degradation 1	9.45	6.65	1.09E−06	8.13E−08
Degradation 2	10.18	7.35	1.18E−06	1.63E−07

[0082] "Standard" denotes a case where no degradation of the OLED occurs, and "Degradation 1" and "Degradation 2" denote the cases where the OLED degrades. The degradation of the OLED is greater in the case of "Degradation 2" than in the case of "Degradation 1."

[0083] As shown in Table 2, as the voltage Vn**4** increases, the voltage Vn**2** increases accordingly. Accordingly, the current flowing through the OLED also increases.

[0084] Since luminous efficiency is lower in the cases where the OLED degrades than in the case where no degradation of the OLED occurs, the current flowing through the OLED is increased so that a gray level that is the same as a gray level represented in the case where no degradation of the OLED occurs is represented in a degraded OLED. Accordingly, based on Table 1 and Table 2, the capacitance cis of the third capacitor Cis is controlled to adjust the voltage variation of the voltage Vn**2**. As a result, the current flowing through the OLED may be controlled.

[0085] FIG. **3** is a circuit diagram of a pixel circuit of a display panel according to another embodiment of the present invention.

[0086] Referring to FIG. **3**, the pixel circuit according to another embodiment includes an OLED, first through sixth transistors M**1** through M**6**, and first through third capacitors C**1**, C**2** and Cis. The connections between these devices are substantially the same as those of the pixel circuit of FIG. **1**. Accordingly, descriptions of the same structure and operation as those of the pixel circuit of FIG. **1** will not be repeated, and the pixel circuit according to another embodiment will now be described by focusing on differences between the pixel circuits of FIGS. **3** and **1**.

[0087] In the embodiment of FIG. **3**, the previous scan signal is applied to the gate electrodes of the second and fourth transistors M**2** and M**4**. Thus, the gate electrodes of the second and fourth transistors M**2** and M**4** are connected to the previous scan line S[N−1].

[0088] The current scan signal is applied to the gate electrode of the fifth transistor M**5**. Accordingly, the gate electrode of the fifth transistor M**5** is connected to the current scan line S[N].

[0089] The emission signal is applied to the gate electrodes of the third and sixth transistors M**3** and M**6**. Accordingly, the gate electrodes of the third and sixth transistors M**3** and M**6** are connected to the emission control line EM[N].

[0090] The first power source provides the first power supply voltage ELVDD, and the second power source provides the second power supply voltage ELVSS. The second power supply voltage ELVSS may be a ground voltage GND. The reference power source may provide the reference voltage Vref, which may be a logic high voltage.

[0091] The operations of the pixel circuits of FIGS. **1** and **3** are substantially the same, and the pixel circuits of FIGS. **1** and **3** operate according to the timing diagram of FIG. **2**. However, in the embodiment of FIG. **3**, the fourth transistor M**4** is first turned on, and the fifth transistor M**5** is then turned on, and thus a current I finally flowing through the OLED is calculated as follows:

$$I=(\beta/2)\{Vref-Vdata+(Voled-Va)(cis/cs)\}^2.$$

[0092] FIG. **4** is a circuit diagram of a pixel circuit of a display panel according to another embodiment of the present invention.

[0093] Referring to FIG. **4**, the pixel circuit according to another embodiment includes an OLED, first through sixth transistors M**1** through M**6**, and first through third capacitors C**1**, C**2** and Cis. The connections between these devices are substantially the same as those of the pixel circuit of FIG. **3**. Accordingly, descriptions of the same structure and operation as those of the pixel circuit of FIG. **3** will not be repeated, and the pixel circuit according to the embodiment of FIG. **4** will now be described by focusing on differences between the pixel circuits of FIGS. **4** and **3**.

[0094] In the embodiment of FIG. **4**, the previous scan signal is applied to the gate electrodes of the second and fourth transistors M**2** and M**4**. Thus, the gate electrodes of the second and fourth transistors M**2** and M**4** are connected to the previous scan line S[N−1].

[0095] The current scan signal is applied to the gate electrode of the fifth transistor M**5**. Accordingly, the gate electrode of the fifth transistor M**5** is connected to the current scan line S[N].

[0096] In the embodiment of FIG. **4**, a clock signal CLK instead of the emission signal is applied to the gate electrodes of the third and sixth transistors M**3** and M**6**. The clock signal CLK may be generated from a system clock. In this case, a special driving unit for generating the emission signal is not used.

[0097] Like the pixel circuit of FIG. **3**, a current I flowing through the OLED of the pixel circuit of FIG. **4** is calculated as follows: $I=(\beta/2)\{Vref-Vdata+(Voled-Va)(cis/cs)\}^2$.

[0098] As described above, in the pixel circuit and the pixel circuit driving method according to the embodiment of FIG. **4**, even if the types of signals applied to the second through sixth transistors M**2** through M**6** are changed, the voltage change of the anode of the OLED caused due to the degradation of the OLED may be reflected in the voltage applied at the gate electrode of the driving transistor M**1** by using the sixth transistor M**6** and the third capacitor Cis. Accordingly, display performance of the display panel including the pixel circuit of FIG. **3** or FIG. **4** may be prevented from degrading.

[0099] FIG. **5** is a circuit diagram of a pixel circuit of a display panel according to another embodiment of the present invention.

[0100] Referring to FIG. **5**, the pixel circuit according to another embodiment includes an OLED, first through seventh transistors M**1** through M**7**, and first through third capacitors C**1**, C**2** and Cis. The connections between these devices are substantially the same as those of the pixel circuit of FIG. **1**. Accordingly, descriptions of the same structure and operation as those of the pixel circuit of FIG. **1** will not be repeated, and the pixel circuit according to the embodiment of FIG. **5** will now be described by focusing on differences between the pixel circuits of FIGS. **5** and **1**.

[0101] In the embodiment of FIG. **5**, the seventh transistor M**7** is further included in addition to the pixel circuit of FIG. **1**.

[0102] The seventh transistor M**7** includes a first electrode connected to the first power source and a second electrode connected to the first electrode of the sixth transistor M**6**. The seventh transistor M**7** also includes a gate electrode to which an external control signal is applied. When the seventh transistor M**7** is turned on by the external control signal, the first power supply voltage ELVDD is applied to the fifth node N**5**. The external control signal may be the current scan signal, which is applied to the gate electrode of the fourth transistor M**4**. Accordingly, the gate electrode of the seventh transistor M**7** is connected to the current scan line S[N].

[0103] The first power source provides the first power supply voltage ELVDD, and the second power source provides the second power supply voltage ELVSS. The second power supply voltage ELVSS may be a ground voltage GND. The reference power source may provide the reference voltage Vref, which may be a ground voltage GND.

[0104] An operation of the pixel circuit of FIG. **5** will now be described with reference to the timing diagram of FIG. **2**.

[0105] In the first interval T**1**, initialization is performed.

[0106] In the first interval T**1**, the previous scan signal is supplied to the previous scan line S[N−1], and the emission signal is supplied to the emission control line EM[N]. In other words, the previous scan signal and the emission signal are logic high in the first interval T**1**. The second, third, fifth, and sixth transistors M**2**, M**3**, M**5**, and M**6** are turned on by the previous scan signal and the emission signal, and thus each node of the pixel circuit is initialized. Here, the current scan signal applied to the current scan line S[N] is logic low.

[0107] In the second interval T**2**, the driving transistor M**1** is diode-connected to compensate for the threshold voltage Vto of the OLED and the threshold voltage Vth of the driving transistor M**1**.

[0108] In the second interval T**2**, the previous scan signal is logic high, and the current scan signal and the emission signal are logic low. According to the previous scan signal, the second and fifth transistors M**2** and M**5** are turned on. When the anode of the OLED is connected to the fourth node N**4** and the threshold voltage of the OLED is Vto, a voltage Vn**4** of the fourth node N**4** is ELVSS+Vto. Since the driving transistor M**1** is diode-connected, a voltage Vn**2** of the second node N**2** is ELVSS+Vto+Vth. A voltage Vn**3** of the third node N**3** becomes the reference voltage Vref. A voltage Vn**5** of the fifth node N**5** is ELVSS+Vto. The voltages of the second to fifth nodes N**2** to N**5** of the pixel circuit of FIG. **5** in the second interval T**2** are summarized as follows.

$N2$: $Vn2=ELVSS+Vto+Vth$

N3: Vn3=Vref

$N4$: $Vn4=ELVSS+Vto$

$N5$: $Vn5=ELVSS+Vto$

[0109] In the third interval T**3**, data writing is performed.

[0110] In the third interval T**3**, the current scan signal is logic high, and the previous scan signal and the emission signal are logic low. When the fourth transistor M**4** is turned on by the current scan signal, the data voltage Vdata is applied to the third node N**3**. In addition, the seventh transistor M**7** is turned on, and thus the first power supply voltage ELVDD is applied to the fifth node N**5**. Voltage changes of the third node N**3** and the fifth node N**5** are reflected in the second node N**2**, and a voltage change of the second node N**2** is calculated as follows. A voltage variation of the voltage Vn**2** according to the voltage change of the third node N**3** is $\Delta V4*\{c1/(c1+cis)\}$, and a voltage variation of the voltage Vn**2** according to the voltage change of the fifth node N**5** is $\Delta V5*\{cis/(c1+cis)\}$. Here, $\Delta V4$ is Vdata−Vref, and $\Delta V5$ is ELVDD-(ELVSS+Vto). The voltages of the second to fifth nodes N**2** to N**5** of the pixel circuit of FIG. **5** in the third interval T**3** are summarized based on this calculation, as follows.

$$N2:\ Vn2 = ELVSS + Vto + Vth + \Delta V4*\{c1/(c1+cis)\} + \Delta V5*\{cis/(c1+cis)\}$$
$$= ELVSS + Vto + Vth + (Vdata - Vref)*\{c1/(c1+cis)\} + \{ELVDD - (ELVSS + Vto)\}*\{cis/(c1+cis)\}$$

$N3$: $Vn3=V\text{data}(\Delta V4=V\text{data}-V\text{ref})$

$N4$: $Vn4=ELVSS+Vto$

$N5$: $Vn5=ELVDD(\Delta V5=ELVDD-(ELVSS+Vto))$

[0111] In the fourth interval T**4**, degradation of the OLED is compensated for. The compensation for the degradation of

the OLED may be achieved by accounting for the voltage change occurring at the anode of the OLED in the voltage applied to the gate electrode of the driving transistor M1.

[0112] In the fourth interval T4, the emission signal is logic high, and the previous scan signal and the current scan signal are logic low. The third and sixth transistors M3 and M6 are turned on by the emission signal. Since the third transistor M3 is turned on, a current flows through the OLED. When the OLED enters into an emission state due to the flow of the current therein, the voltage Vn4 of the fourth node N4, which is connected to the anode of the OLED, is changed. When a voltage between the anode and cathode of the OLED during light emission is Voled, the voltage Vn4 is ELVSS+Voled. The voltage Voled varies according to the degree of degradation of the OLED. When the sixth transistor M6 is turned on, the voltages Vn4 and Vn5 of the fourth and fifth nodes N4 and N5 are changed to ELVSS+Voled, and thus the voltage Vn2 of the second node N2 is also changed. In other words, the third capacitor Cis and the sixth transistor M6 serve as a boost capacitor and a boost transistor, respectively. In calculating the voltage change of the voltage Vn2, a voltage variation of the voltage Vn2 depending on the voltage change of the fourth node N4 is ΔV6*{cs/(cs+cis)} and a voltage variation of the voltage Vn2 depending on the voltage change of the fifth node N5 is ΔV7*{cis/(cs+cis)}, where ΔV6=Voled−Vto, ΔV7=ELVSS+Voled-ELVDD, and cs denotes a composite capacitance when the first and second capacitors C1 and C2 are connected to each other in series. The voltages of the second, fourth and fifth nodes N2, N4 and N5 of the pixel circuit of FIG. 5 are summarized based on this calculation, as follows.

$$N2:\ Vn2 = ELVSS + Vto + Vth + (Vdata - Vref) * \{c1/(c1+cis)\} + \{ELVDD - (ELVSS + Vto)\} * \{cis/(c1+cis)\} + (Voled - Vto) * \{cs/(cs+cis)\} + (ELVSS + Voled - ELVSS) * \{cis/(cs+cis)\}$$

$$N4:\ Vn4 = ELVSS + Voled(\Delta V6 = Voled - Vto)$$

$$N5:\ Vn5 = ELVSS + Voled(\Delta V7 = ELVSS + Voled - ELVDD)$$

[0113] The voltage Vn2 of the second node N2 is the voltage of the gate electrode of the driving transistor M1, and the voltage Vn4 of the fourth node N4 is the voltage of the source electrode of the driving transistor M1. In view of a condition of c1, c2>>cis, cs>>cis, accordingly,

$$\begin{aligned} Vg &= Vn2 \\ &\approx ELVSS + Vto + Vth + Vdata - Vref + (Voled - Vto) + (ELVSS + Voled - ELVDD) * \{cis/cs\} \\ &= ELVSS + Vth + Vdata - Vref + Voled + (ELVSS + Voled - ELVDD) * \{cis/cs\} \\ Vs &= Vn4 \\ &= ELVSS + Voled \end{aligned}$$

[0114] A current I flowing through the OLED according to the voltages of the driving transistor M1 is calculated as follows:

$$\begin{aligned} I &= (\beta/2)(Vgs - Vth)^2 \\ &= (\beta/2)(Vg - Vs - Vth)^2 \\ &= (\beta/2)\left\{ \begin{array}{c} ELVSS + Vth + Vdata - Vref + Voled + \\ (ELVSS + Voled - ELVDD)(cis/cs) - \\ (ELVSS + Voled) - Vth \end{array} \right\}^2 \\ &= (\beta/2)\{Vdata - Vref + (ELVSS + Voled - ELVDD)(cis/cs)\}^2, \end{aligned}$$

wherein β denotes a gain factor.

[0115] With the above-described current I flowing through the OLED, it may be known that the voltage Voled varying according to the degradation of the OLED is reflected in the current I.

[0116] As described above, in the pixel circuit and the pixel circuit driving method according to the embodiment of FIG. 5, the voltage change of the anode of the OLED caused due to the degradation of the OLED may be reflected in the voltage applied to the gate electrode of the driving transistor M1 by using the sixth and seventh transistors M6 and M7 and the third capacitor Cis. Accordingly, display performance of the display panel including the pixel circuit of FIG. 5 may be prevented from degrading.

[0117] Table 3 shows a result of a simulation performed on the pixel circuit of FIG. 5.

TABLE 3

	Before degradation	After degradation
Vn5(V)	−6.03	−4.59
Vn2(V)	1.69	2.3

[0118] As shown in Table 3, the voltage Vn5 increases as the OLED degrades, and the voltage Vn2 increases as the voltage Vn5 increases.

[0119] Table 4 shows a result of another simulation performed on the pixel circuit of FIG. 5.

TABLE 4

	Vn2(V)	Vn4(V)	I(A)	ΔI(A)
Standard	8.71	5.69	1.01E−06	0.00E+00
Degradation 1	9.49	6.68	1.12E−06	1.13E−07
Degradation 2	10.27	7.41	1.24E−06	2.27E−07

[0120] "Standard" denotes a case where no degradation of the OLED occurs, and "Degradation 1" and "Degradation 2" denote the cases where the OLED degrades. The Degradation of the OLED is greater in the case of "Degradation 2" than in the case of "Degradation 1".

[0121] As shown in Table 4, as the voltage Vn4 increases, the voltage Vn2 increases accordingly. Accordingly, the current flowing through the OLED also increases.

[0122] Since luminous efficiency is lower in the cases where the OLED degrades than in the case where no degradation of the OLED occurs, the current flowing through the OLED is increased so that a gray level that is the same as a gray level represented in the case where no degradation of the

OLED occurs is represented in a degraded OLED. Accordingly, based on Table 3 and Table 4, the capacitance cis of the third capacitor Cis is controlled to adjust the voltage variation of the voltage Vn2. As a result, the current flowing through the OLED may be controlled.

[0123] FIG. **6** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention.

[0124] Referring to FIG. **6**, the pixel circuit according to another embodiment includes an OLED, first through seventh transistors M1 through M7, and first through third capacitors C1, C2 and Cis. The connections between these devices are substantially the same as those of the pixel circuit of FIG. **5**. Accordingly, descriptions of the same structure and operation as those of the pixel circuit of FIG. **5** will not be repeated, and the pixel circuit according to the embodiment of FIG. **6** will now be described by focusing on differences between the pixel circuits of FIGS. **6** and **5**.

[0125] In the embodiment of FIG. **6**, the previous scan signal is applied to the gate electrodes of the second and fourth transistors M2 and M4. Thus, the gate electrodes of the second and fourth transistors M2 and M4 are connected to the previous scan line S[N−1].

[0126] The current scan signal is applied to the gate electrodes of the fifth and seventh transistors M5 and M7. Accordingly, the gate electrodes of the fifth and seventh transistors M5 and M7 are connected to the current scan line S[N].

[0127] The emission signal is applied to the gate electrodes of the third and sixth transistors M3 and M6. Accordingly, the gate electrodes of the third and sixth transistors M3 and M6 are connected to the emission control line EM[N].

[0128] The first power source provides the first power supply voltage ELVDD, and the second power source provides the second power supply voltage ELVSS. The second power supply voltage ELVSS may be a ground voltage GND. The reference power source may provide the reference voltage Vref, which may be a logic high voltage.

[0129] The operations of the pixel circuits of FIGS. **5** and **6** are substantially the same, and the pixel circuits of FIGS. **5** and **6** operate according to the timing diagram of FIG. **2**. However, in the embodiment of FIG. **6**, the fourth transistor M4 is first turned on, and the fifth transistor M5 is then turned on, and thus a current I finally flowing through the OLED is calculated as follows:

$$I=(\beta/2)\{Vref-Vdata+(ELVSS+Voled-ELVDD)(cis/cs)\}^2.$$

[0130] FIG. **7** is a circuit diagram of a pixel circuit of a display panel, according to another embodiment of the present invention.

[0131] Referring to FIG. **7**, the pixel circuit according to another embodiment includes an OLED, first through seventh transistors M1 through M7, and first through third capacitors C1, C2 and Cis. The connections between these devices are substantially the same as those of the pixel circuit of FIG. **6**. Accordingly, descriptions of the same structure and operation as those of the pixel circuit of FIG. **6** will not be repeated, and the pixel circuit according to the embodiment of FIG. **7** will now be described by focusing on differences between the pixel circuits of FIGS. **7** and **6**.

[0132] In the embodiment of FIG. **7**, the previous scan signal is applied to the gate electrodes of the second and fourth transistors M2 and M4. Thus, the gate electrodes of the second and fourth transistors M2 and M4 are connected to the previous scan line S[N−1].

[0133] The current scan signal is applied to the gate electrodes of the fifth and seventh transistors M5 and M7. Accordingly, the gate electrodes of the fifth and seventh transistors M5 and M7 are connected to the current scan line S[N].

[0134] In the embodiment of FIG. **7**, a clock signal CLK instead of the emission signal is applied to the gate electrodes of the third and sixth transistors M3 and M6. The clock signal CLK may be generated from a system clock. In this case, a special driving unit for generating the emission signal is not used.

[0135] Like the pixel circuit of FIG. **6**, a current I flowing through the OLED of the pixel circuit of FIG. **7** is calculated as follows:

$$I=(\beta/2)\{Vref-Vdata+(ELVSS+Voled-ELVDD)(cis/cs)\}^2.$$

[0136] As described above, in the pixel circuit and the pixel circuit driving method according to the embodiment of FIG. **7**, even if the types of signals applied to the second through sixth transistors M2 through M6 are changed, the voltage change of the anode of the OLED caused due to the degradation of the OLED may be reflected in the voltage applied at the gate electrode of the driving transistor M1 by using the sixth and seventh transistors M6 and M7 and the third capacitor Cis. Accordingly, display performance of the display panel including the pixel circuit of FIG. **6** or FIG. **7** may be prevented from degrading.

[0137] FIG. **8** is a block diagram of an organic light emitting display device **100** according to an embodiment of the present invention.

[0138] Referring to FIG. **8**, the organic light emitting display device **100** according to an embodiment includes a display panel **110**, a scan driving unit **120**, a data driving unit **130**, and an emission driving unit **140**.

[0139] The display panel **110** includes n×m pixels, n scan lines S[1] . . . S[n] arranged in rows, m data lines D[1] . . . D[m] arranged in columns, n emission control lines EM[1] . . . EM[n] arranged in rows, a first power supply voltage (ELVDD) application wire, and a second power supply voltage (ELVSS) application wire. Any of the pixel circuits of FIGS. **1** and **3-7** may be formed in each of the pixels.

[0140] The scan lines S[1] . . . S[n] transmit scan signals to the pixels. The data lines D[1] . . . D[m] transmit data signals to the pixels.

[0141] The scan driving unit **120** supplies the scan signals to the scan lines S[1] . . . S[n]. The scan signals are sequentially applied to the scan lines S[1] . . . S[n], and the data signals are applied to the pixels in accordance with the scan signals.

[0142] The data driving unit **130** applies the data signals to the data lines D[1] . . . D[m]. The data signals may be output from a voltage source or a current source included in the data driving unit **130**.

[0143] The emission driving unit **140** applies emission signals to the emission control lines EM[1] . . . EM[n].

[0144] Timings of the scan signals and the emission signals may be the same as those of the timing diagram of FIG. **2**.

[0145] The pixels may be formed at crossing regions between the scan lines S[1] . . . S[n], the data lines D[1] . . . D[m], and the emission control lines EM[1] . . . EM[n].

[0146] As described above, the organic light emitting display device **100** according to one embodiment includes pixel circuits that can compensate for degradation of OLEDs, thereby preventing reduction of display performance.

[0147] A program for executing methods of driving pixel circuits according to the above-described embodiments and other embodiments may be stored in storage media. The storage media may include magnetic storage media (e.g., ROMs, floppy disks, hard disk, and the like) and optical storage media (e.g., CD ROMS, DVDs and the like).

[0148] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims and their equivalents.

What is claimed is:

1. A pixel circuit for a display panel, comprising:

an organic light emitting diode (OLED) comprising an anode and a cathode;

a first NMOS transistor comprising a first electrode coupled to a first node, a second electrode coupled to the anode of the OLED, and a gate electrode coupled to a second node;

a second NMOS transistor comprising a first electrode coupled to the second node, a second electrode coupled to the first node, and a gate electrode;

a third NMOS transistor comprising a first electrode coupled to a first power source, a second electrode coupled to the first node, and a gate electrode;

a fourth NMOS transistor comprising a first electrode coupled to a data line, a second electrode coupled to a third node, and a gate electrode;

a fifth NMOS transistor comprising a first electrode coupled to a reference power source, a second electrode coupled to the third node, and a gate electrode;

a sixth NMOS transistor comprising a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode;

a first capacitor coupled between the second node and the third node;

a second capacitor coupled between the third node and the anode of the OLED; and

a third capacitor coupled between the second node and the first electrode of the sixth NMOS transistor.

2. The pixel circuit of claim **1**, wherein the gate electrode of the second NMOS transistor and the gate electrode of the fifth NMOS transistor are configured to receive a previous scan signal.

3. The pixel circuit of claim **2**, wherein the gate electrode of the fourth NMOS transistor is configured to receive a current scan signal.

4. The pixel circuit of claim **3**, wherein the gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor are configured to receive an emission signal.

5. The pixel circuit of claim **4**, further comprising a seventh NMOS transistor comprising a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode configured to receive the current scan signal.

6. The pixel circuit of claim **5**, wherein the reference power source has a ground voltage.

7. The pixel circuit of claim **1**, wherein the gate electrode of the second NMOS transistor and the gate electrode of the fourth NMOS transistor are configured to receive a previous scan signal.

8. The pixel circuit of claim **7**, wherein the gate electrode of the fifth NMOS transistor is configured to receive a current scan signal.

9. The pixel circuit of claim **8**, wherein the gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor are configured to receive an emission signal.

10. The pixel circuit of claim **8**, wherein the gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor are configured to receive an external clock signal.

11. The pixel circuit of claim **9**, further comprising a seventh NMOS transistor comprising a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode configured to receive the current scan signal.

12. The pixel circuit of claim **11**, wherein the reference power source has a logic high signal.

13. The pixel circuit of claim **1**, wherein the first electrode of the first NMOS transistor comprises a drain electrode and the second electrode of the first NMOS transistor comprises a source electrode.

14. The pixel circuit of claim **1**, wherein capacitances of the first and second capacitors are greater than capacitance of the third transistor.

15. A method of driving a pixel circuit comprising an OLED having an anode and a cathode, a driving transistor, a plurality of switching transistors, a booster transistor having a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode, a plurality of capacitors, and a booster capacitor coupled between the gate electrode of the driving transistor and the first electrode of the booster transistor,

wherein the driving transistor, the plurality of switching transistors and the booster transistor are NMOS transistors, the method comprising:

turning on the booster transistor when a previous scan signal and a current scan signal are logic low and an emission signal is logic high; and

transmitting a voltage change at the anode of the OLED to the gate electrode of the driving transistor via coupling of the booster capacitor.

16. The method of claim **15**, wherein the voltage change at the anode of the OLED corresponds to a voltage difference between a voltage at the anode when substantially no current flows through the OLED and a voltage at the anode when a current flows through the OLED.

17. The method of claim **15**, further comprising initializing the pixel circuit when the previous scan signal and the emission signal are logic high and the current scan signal is logic low.

18. The method of claim **15**, further comprising diode-connecting the driving transistor to compensate for a threshold voltage of the OLED when the previous scan signal is logic high and the current scan signal and the emission signal are logic low.

19. The method of claim **15**, further comprising performing data writing when the previous scan signal and the emission signal are logic low and the current scan signal is logic high.

20. An organic light emitting display device comprising:

a scan driver for providing scan signals to a plurality of scan lines;

an emission driver for providing emission signals to a plurality of emission control lines;

a data driver for providing data signals to a plurality of data lines; and

a plurality of pixel circuits at crossing regions between the scan lines, the emission control lines, and the data lines,

wherein each of the pixel circuits comprises:

an organic light emitting diode (OLED) comprising an anode and a cathode;

a first NMOS transistor comprising a first electrode coupled to a first node, a second electrode coupled to the anode of the OLED, and a gate electrode coupled to a second node;

a second NMOS transistor comprising a first electrode coupled to the second node, a second electrode coupled to the first node, and a gate electrode;

a third NMOS transistor comprising a first electrode coupled to a first power source, a second electrode coupled to the first node, and a gate electrode;

a fourth NMOS transistor comprising a first electrode coupled to a data line, a second electrode coupled to a third node, and a gate electrode;

a fifth NMOS transistor comprising a first electrode coupled to a reference power source, a second electrode coupled to the third node, and a gate electrode;

a sixth NMOS transistor comprising a first electrode, a second electrode coupled to the anode of the OLED, and a gate electrode;

a first capacitor coupled between the second node and the third node;

a second capacitor coupled between the third node and the anode of the OLED; and

a third capacitor coupled between the second node and the first electrode of the sixth NMOS transistor.

21. The organic light emitting display device of claim **20**, wherein:

the gate electrode of the second NMOS transistor and the gate electrode of the fifth NMOS transistor are connected to an (N−1)th scan line;

the gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor are coupled to an N-th emission control line; and

the gate electrode of the fourth NMOS transistor is coupled to an N-th scan line.

22. The organic light emitting display device of claim **20**, wherein:

the gate electrode of the second NMOS transistor and the gate electrode of the fourth NMOS transistor are coupled to an (N−1)th scan line;

the gate electrode of the third NMOS transistor and the gate electrode of the sixth NMOS transistor are coupled to an N-th emission control line; and

the gate electrode of the fifth NMOS transistor is coupled to an N-th scan line.

23. The organic light emitting display device of claim **21**, further comprising a seventh NMOS transistor comprising a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode coupled to the N-th scan line.

24. The organic light emitting display device of claim **22**, further comprising a seventh NMOS transistor comprising a first electrode coupled to the first power source, a second electrode coupled to the first electrode of the sixth NMOS transistor, and a gate electrode coupled to the N-th scan line.

25. The organic light emitting display device of claim **20**, wherein the first electrode of the first NMOS transistor comprises a drain electrode and the second electrode of the first NMOS transistor comprises a source electrode.

26. The organic light emitting display device of claim **20**, wherein capacitances of the first and second capacitors are greater than capacitance of the third transistor.

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专利名称(译)	显示面板的像素电路，控制像素电路的方法，以及包括显示面板的有机发光显示器		
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[标]申请(专利权)人(译)	众博YONG KIM KEUM NAM		
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当前申请(专利权)人(译)	众博勇 KIM KEUM-NAM		
[标]发明人	CHUNG BO YONG KIM KEUM NAM		
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摘要(译)

提供显示面板的像素电路，驱动像素电路的方法，以及包括该显示面板的有机发光显示装置。在像素电路中使用的所有多个晶体管都是NMOS晶体管，并且像素电路被配置为在发光期间补偿驱动晶体管的源电极处的电压变化。